ALPHA & OMEGA SEMICONDUCTOR

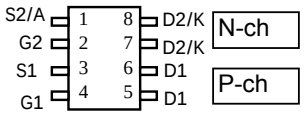
AOP610
Complementary Enhancement Mode Field Effect Transistor

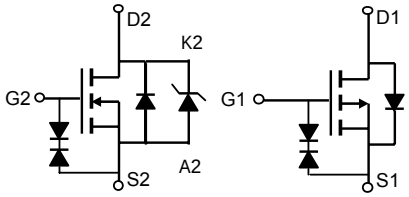
General Description
The AOP610 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications. A Schottky diode in parallel with the n-channel FET reduces body diode related losses. It is ESD protected. *Standard product AOP610 is Pb-free (meets ROHS & Sony 259 specifications). AOP610L is a Green Product ordering option. AOP610 and AOP610L are electrically identical.*

Features
n-channel	p-channel
V_{DS} (V) = 30V	-30V
I_D = 7.7A (V_{GS}=10V)	-6.2A (V_{GS}=10V)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 24mΩ (V_{GS}=10V)	< 39mΩ (V_{GS} = -10V)
< 42mΩ (V_{GS}=4.5V)	< 56mΩ (V_{GS} = -4.5V)

ESD rating: 2000V (HBM)

PDIP-8





n-channel **p-channel**

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current [A]	T_A=25°C	I_D	7.7	-6.2	A
	T_A=70°C		6.1	-4.9	
Pulsed Drain Current [B]		I_{DM}	30	-30	
Power Dissipation	T_A=25°C	P_D	2.3	2.3	W
	T_A=70°C		1.45	1.45	
Avalanche Current [B]		I_{AR}	10	15	A
Repetitive avalanche energy 0.3mH [B]		E_{AR}	15	33	mJ
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	-55 to 150	°C

Thermal Characteristics: n-channel+schottky and p-channel

Parameter		Symbol	Typ	Max		Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	n-ch	45	55	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		n-ch	78	95	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	n-ch	30	40	°C/W
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	p-ch	38.5	55	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		p-ch	78	95	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	p-ch	28	40	°C/W

N-Channel+Schottky Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0V		2	50	µA
		T_J=55°C			125	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V			10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1	2	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	20			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=7.7A		20	24	mΩ
		T_J=125°C		29	35	
		V_{GS}=4.5V, I_D=4A		32	42	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=7.7A	10	18		S
V_{SD}	Diode Forward Voltage	I_S=1A		0.5	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		543	630	pF
C_{oss}	Output Capacitance			142		pF
C_{rss}	Reverse Transfer Capacitance			76		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		2.1	3	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=7.7A		11	15	nC
Q_g(4.5V)	Total Gate Charge			5.3	7	nC
Q_{gs}	Gate Source Charge			1.9		nC
Q_{gd}	Gate Drain Charge			4		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.9Ω, R_{GEN}=3Ω		4.7	7	ns
t_r	Turn-On Rise Time			4.9	10	ns
$t_{D(off)}$	Turn-Off DelayTime			16.2	22	ns
t_f	Turn-Off Fall Time			3.5	7	ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=7.7A, dI/dt=100A/µs		15.7	20	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=7.7A, dI/dt=100A/µs		7.9	10	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient. $R_{\theta JL}$ and $R_{\theta JC}$ are equivalent terms referring to thermal resistance from junction to drain lead.

D. The static characteristics in Figures 1 to 6 are obtained using 80µs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F. Rev 3: Jul 2006

N-CH+SCHOTTKY TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

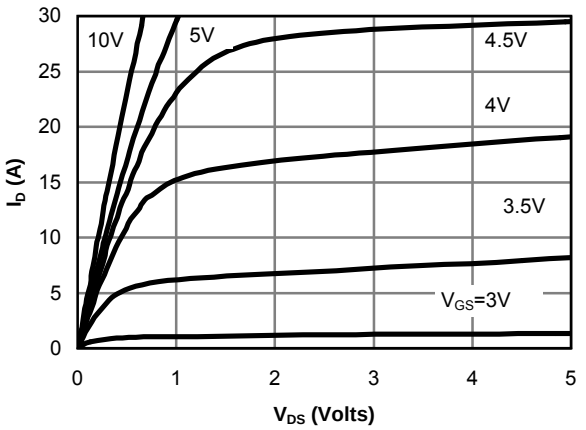


Fig 1: On-Region Characteristics

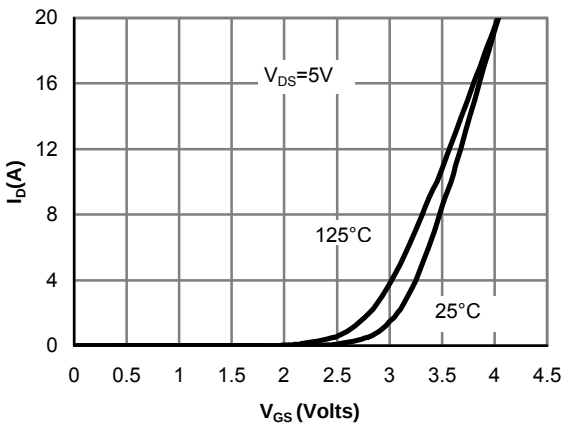


Figure 2: Transfer Characteristics

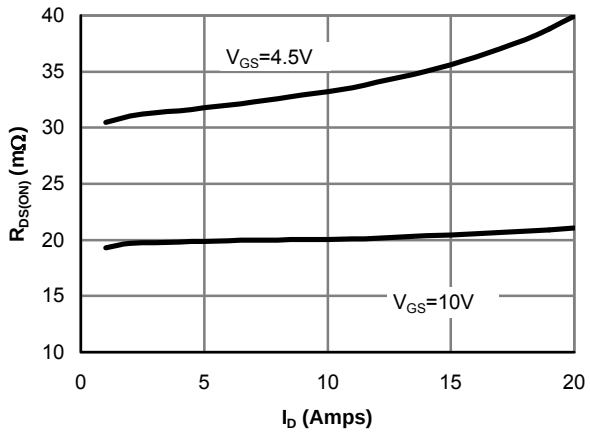


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

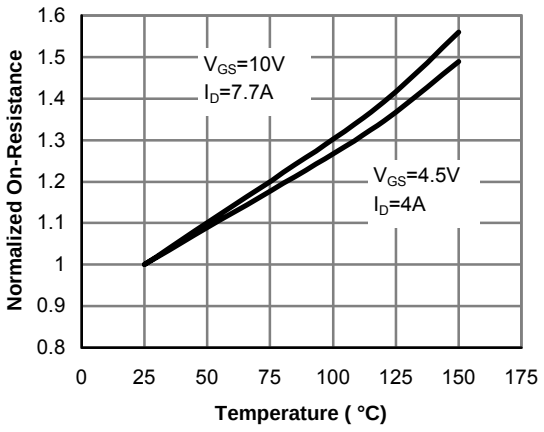


Figure 4: On-Resistance vs. Junction Temperature

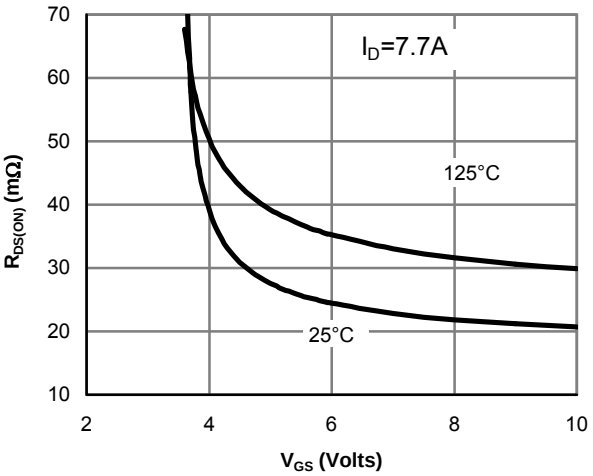


Figure 5: On-Resistance vs. Gate-Source Voltage

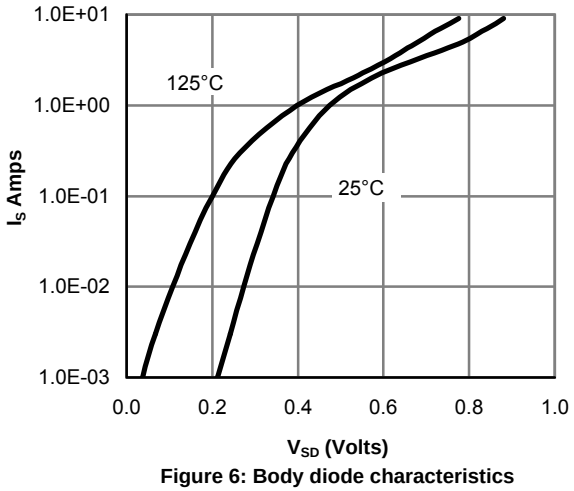


Figure 6: Body diode characteristics

N-CH+SCHOTTKY TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

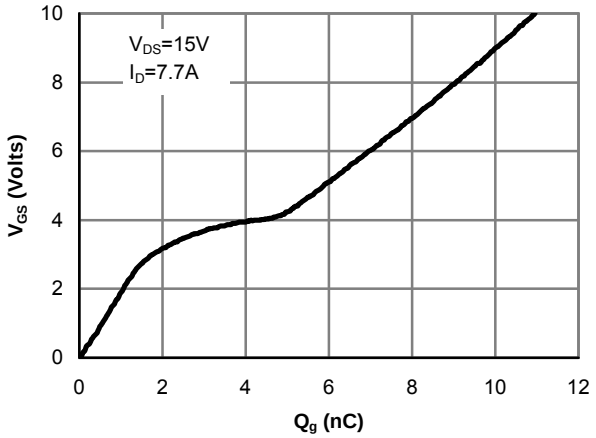


Figure 7: Gate-Charge characteristics

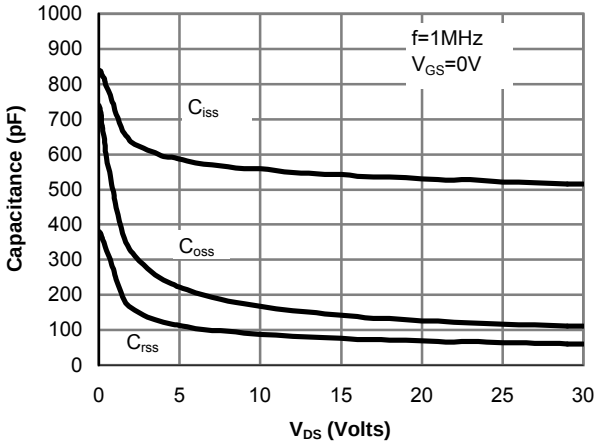


Figure 8: Capacitance Characteristics

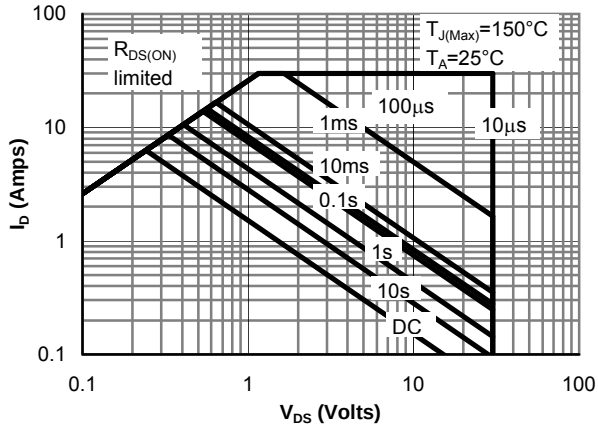


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

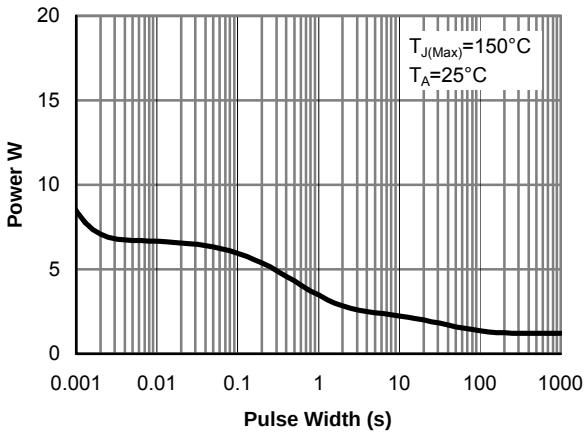


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

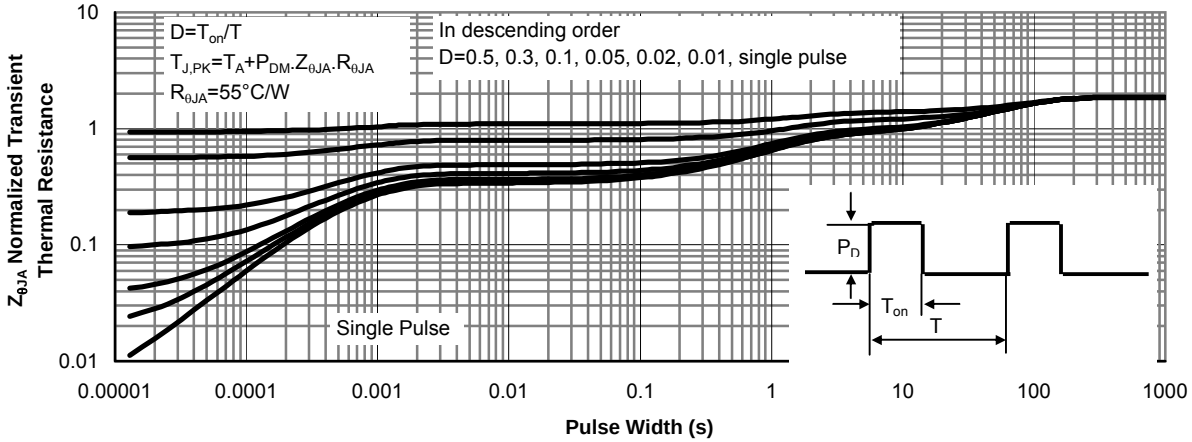


Figure 11: Normalized Maximum Transient Thermal Impedance

P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V			-1	µA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V			10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-1	-1.8	-3	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-6.2A		32	39	mΩ
		T_J=125°C		43	52	
		V_{GS}=-4.5V, I_D=4A		45	56	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-6.2A		12.5		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.77	-1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		1040	1250	pF
C_{oss}	Output Capacitance			179		pF
C_{rss}	Reverse Transfer Capacitance			134		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		5	10	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge (10V)	V_{GS}=-10V, V_{DS}=-15V, I_D=-6.2A		16.8	22	nC
Q_g(4.5V)	Total Gate Charge (4.5V)			8.7	12	nC
Q_{gs}	Gate Source Charge			3.4		nC
Q_{gd}	Gate Drain Charge			5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=2.5Ω, R_{GEN}=3Ω		9	12	ns
t_r	Turn-On Rise Time			5.7	11	ns
$t_{D(off)}$	Turn-Off DelayTime			22.7	30	ns
t_f	Turn-Off Fall Time			10.2	20	ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-6.2A, dI/dt=100A/µs		21.7	27	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-6.2A, dI/dt=100A/µs		13.6	18	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

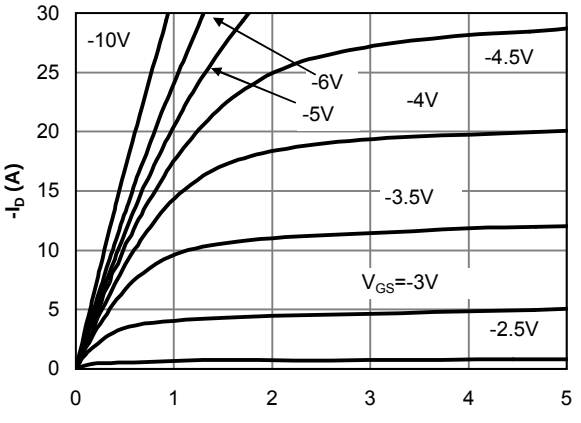
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient. $R_{\theta JL}$ and $R_{\theta JC}$ are equivalent terms referring to thermal resistance from junction to drain lead.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80µs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F. Rev 3: Jul 2006

P-CH TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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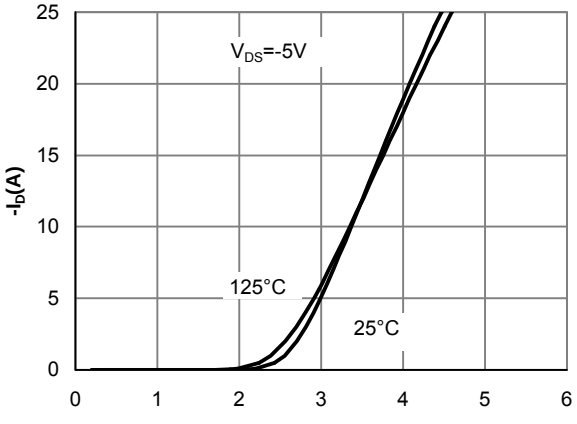


Figure 2: Transfer Characteristics

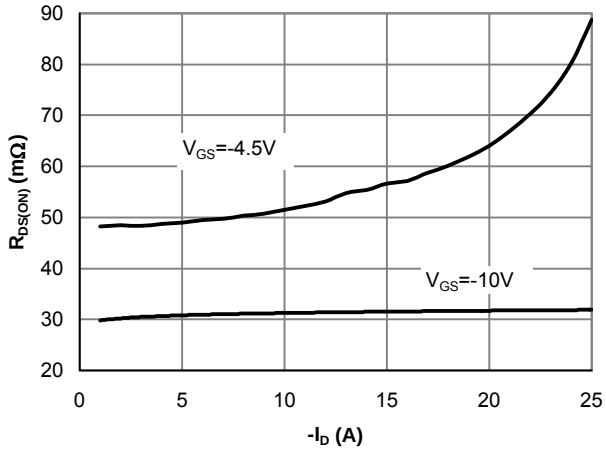


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

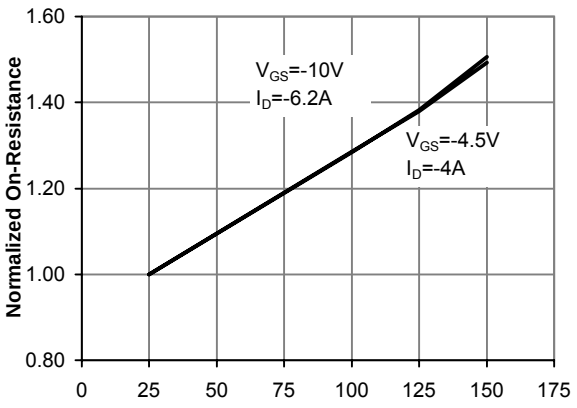
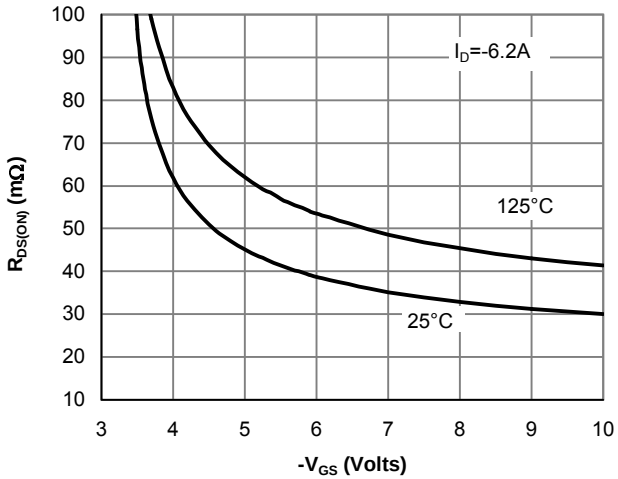


Figure 4: On-Resistance vs. Junction Temperature



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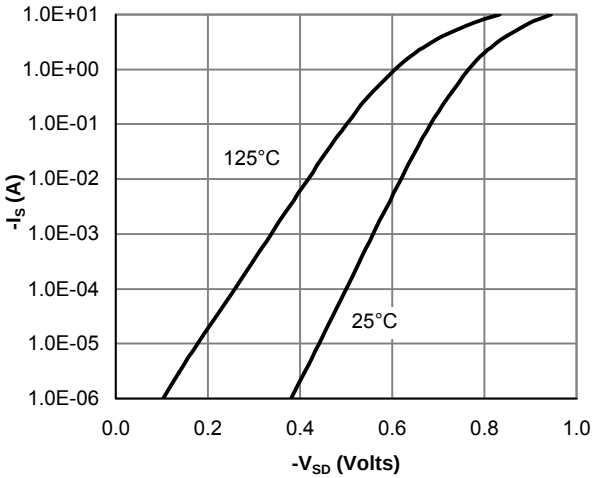

Figure 6: Body-Diode Characteristics

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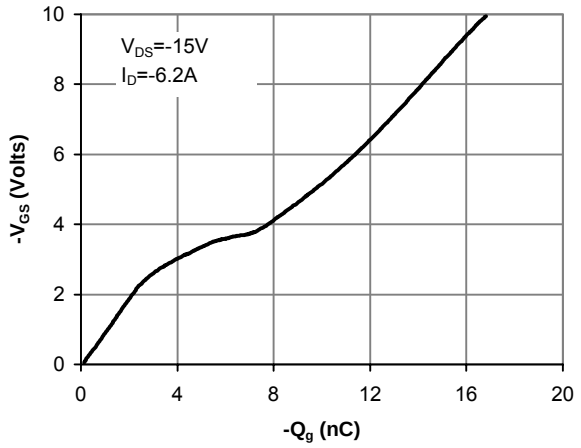
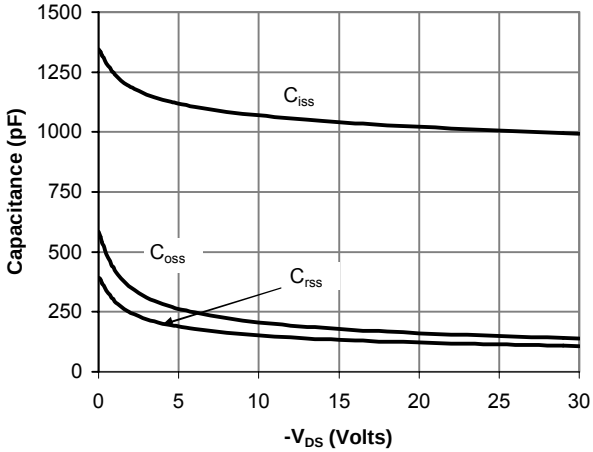


Figure 7: Gate-Charge Characteristics



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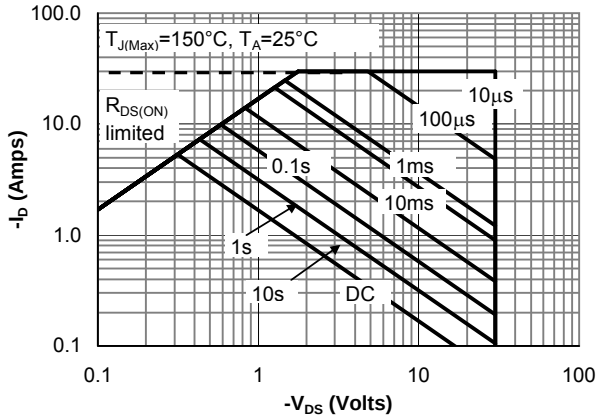

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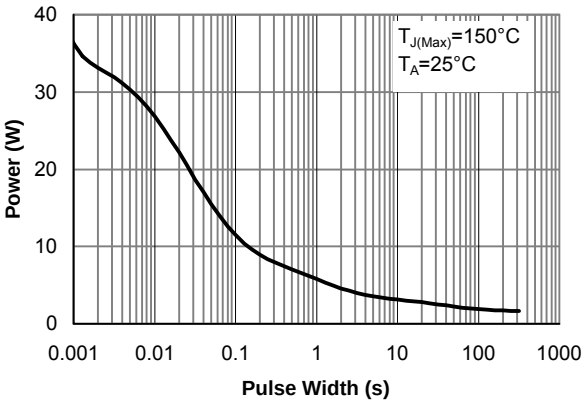

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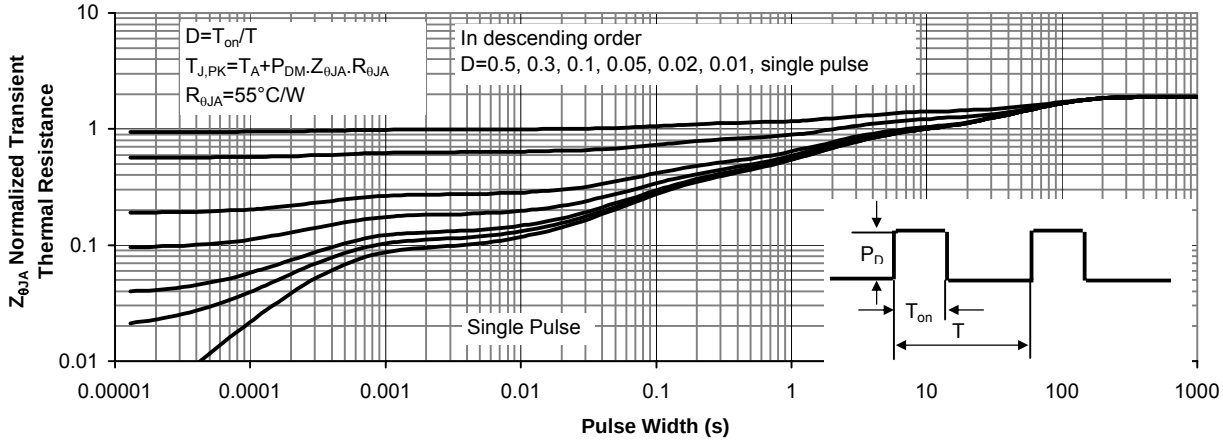

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